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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,001	12/30/2003	Sung-Kwon Lee	51876P507	9960

8791 7590 01/26/2007

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EXAMINER	
JEFFERSON, QUOVAUNDA	
ART UNIT	PAPER NUMBER
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,001	LEE ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29,31,32 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29,31,32 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

1. Claims 12-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no description in the specification as originally filed of "an attack barrier layer formed between the second plug and the conductive patterns removes a gap formed when the second contact hole is formed". There is only seen description of "an attack barrier layer formed between the second plug and the conductive patterns removes a gap which occurred during the cleaning process", which is recited on page 21, lines 4-5

2. Claims 12-18 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "an attack barrier layer formed the second plug and the conductive patterns removes a gap which occurred during the cleaning process", does not reasonably provide enablement for of "an attack barrier layer formed between the second plug and the conductive patterns removes a gap formed when the second contact hole is formed".

The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. There is no description of "an attack barrier layer formed between the second plug and the conductive patterns removes a gap formed when the second contact hole is formed" discussed above and therefore insufficient guidance to enable one of ordinary skill in the art to determine suitable process to achieve the instant application.

3. Claims 12-18 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 12 recites the limitation "an attack barrier layer formed between the second plug and the conductive patterns removes a gap formed when the second contact hole is formed"; the attack barrier layer being formed over a resulting structure.

However, drawings 3A, 3B, 3C, and 3D clearly show that the attack barrier layer **31** removes gaps **A** formed before the second contact hole **30** is formed. Page 6, lines 2-4 of Applicant's Specification recites that these gaps are the result of a partial loss of an upper portion of the oxide layer by the cleaning process, this attack barrier layer fills in the gap portions that were lost during the cleaning process that was done prior to the formation of the second contact hole.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11, 31, 32, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein referred to as AAPA) in view of Tran, US Patent 5,942,801.

5. Regarding claim 1, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer structure along a profile containing conductive patterns **G** formed on a substrate, etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate

allocated between the conductive patterns (Figure 1A), forming a first plug **17** by depositing a conductive layer on an entire surface of the resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns (Figure 1B), performing a cleaning process to remove remnants from the planarization process (page 5, lines 6-19), etching selectively a second inter-layer insulation layer **18** deposited along a profile containing the first plug to form a second contact hole exposing the first plug (Figure 1C); and forming a second plug electrically connected to the first plug through the second contact hole (Figure 1D).

AAPA fails to teach forming an attack barrier layer above the etch stop layer exposed by the second contact hole, wherein the attack barrier layer removes a gap formed when the second contact hole is formed.

Tran teaches forming an attack barrier layer **67** above the etch stop layer **63, 64** exposed by the second contact hole, wherein a lost portion of the etch stop layer is filled with a portion of the attack barrier layer (figure 6 and column 6, lines 37-40) because the barrier layer serves as an adhesion promoter for the conductive plug material to be added and prevents the reaction of the conductive plug and the semiconductor layers.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Tran with that of AAPA because the barrier layer serves as an

adhesion promoter for the conductive plug material to be added and prevents the reaction of the conductive plug and the semiconductor layers.

6. Regarding claim 2, AAPA teaches the multilayer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating material-based layer being disposed between the nitride layer and having a lower dielectric constant than those of the nitride layers (page 2, line 22).

7. Regarding claim 3, AAPA teaches the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole (page 4, lines 1-25).

8. Regarding claim 4, AAPA and Tran fail to teach the thickness of the first inter layer insulation layer and the etch stop layer disposed on each conductive pattern ranges from about 500 Angstroms to about 1500 Angstroms. However, given the teaching of the references, it would have been obvious to determine the optimum thickness of the semiconductor layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another

variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

9. Regarding claim 5, Tran teaches after the step of performing the cleaning process, the attack barrier layer **67** is deposited on an entire surface of the profile containing the first plug (column 6, lines 28 and 37-40).

10. Regarding claim 6, Tran teaches after the step of forming the second contact hole, the attack barrier layer is formed along a profile containing the second contact hole (figure 6).

11. Regarding claim 7, Tran teaches the attack barrier layer is a nitride-based layer (column 6, line 43).

12. Regarding claim 8, AAPA and Tran fail to teach the attack barrier layer has a thickness ranging from about 50 A to about 500 A . However, given the teaching of the references, it would have been obvious to determine the optimum thickness of the semiconductor layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re* Woodruff, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka,* 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 9, AAPA teaches the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_2O_3) layer and a tantalum oxynitride (TaON) layer (page 2, line 22).

Regarding claim 10, AAPA teaches the cleaning process uses a cleaning solution of hydrofluoric acid (HF) or buffered oxide etchant (BOE) (page 5, lines 19).

Regarding claim 11, AAPA teaches the conductive pattern **G** is a gate electrode pattern and the second plug **22** is a storage node contact plug (page 2, line 26 and page 8, line 9).

Regarding claim 31, AAPA teaches the second inter-layer insulation layer has a flow-fill property (page 4, line 22 to page 5, line 11).

Regarding claim 32, AAPA teaches the second inter-layer insulation layer is made of an oxide-based material selected from a group consisting of advanced

planarization layer (APL), spin on dielectric (SOD), spin on glass (SOG) and borophosphosilicate glass (BPSG) (page 4, line 22 to page 5, line 11).

Regarding claim 36, AAPA and Tran fail to teach the second inter-layer insulation layer has a thickness ranging from about 1000 A to about 8000 Angstroms. However, given the teaching of the references, it would have been obvious to determine the optimum thickness of the semiconductor layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Claims 21-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (herein referred to as "AAPA") in view of Jiang, US Patent Application Publication 2002/0055256.

Regarding claim 21, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer structure along a profile containing conductive patterns **G** formed on a substrate (Figure 1A), etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (Figure 1 A), forming a first plug **17** by depositing a conductive layer on an entire surface of a structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns and the first inter-layer insulation layer by employing a CMP process, performing a cleaning process to remove remnants from the planarizing process (page 5, lines 6-19) and etching selectively a second inter-layer insulation layer deposited on the resulting structure including the first plug to form a second contact hole exposing the first plug (Figure 1 C),

AAPA fails to teach forming an attack barrier layer along a profile containing the second contact hole, removing the attack barrier layer disposed at a bottom surface of the second contact hole through an etch-back process and forming a second plug electrically connected to the first plug through the second contact hole, wherein an attack barrier layer formed between the second plug and the conductive pattern removes a gap formed when the second contact hole is formed.

Jiang teaches forming an attack barrier layer **110** along a profile containing the second contact hole (figure 3A), removing the attack barrier layer disposed at a bottom surface of the second contact hole through an etch-back process (figure 3C) and forming a second plug **114** electrically connected to the first plug **105** through the second contact hole, wherein an attack barrier layer formed between the second plug and the conductive pattern removes a gap formed when the second contact hole is formed (figure 3D) because the attack barrier layer, or dielectric liner, smoothes the sidewalls of the trench, thereby filling in the gaps from the roughened surface of the trench sidewall from the etching to form said trench. The advantage of this dielectric thin film is to repair the rough sidewall to reduce the copper line resitivity, thereby making the flow of electricity easier in the semiconductor device.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Jiang with that of AAPA because the attack barrier layer, or dielectric liner, smoothes the sidewalls of the trench, thereby filling in the gaps from the

roughened surface of the trench sidewall from the etching to form said trench. The advantage of this dielectric thin film is to repair the rough sidewall to reduce the copper line resitivity, thereby making the flow of electricity easier in the semiconductor device.

Regarding claim 22, AAPA teaches the multi-layer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating material-based layer being disposed between the nitride layers and having a lower dielectric constant than those of the nitride layers (page 2, line 22).

Regarding claim 23, AAPA teaches the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole (page 4, lines 1-25).

Regarding claim 24, AAPA and Jiang fail to teach the thickness of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern preferably ranges from about 500 Angstroms to about 1500 Angstroms. However, given the teaching of the references, it would have been obvious to determine the optimum thickness of the semiconductor layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical

nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 25, Jiang teaches the attack barrier layer is a nitride-based layer [0025].

Regarding claim 26, Jiang teaches the attack barrier layer has a thickness ranging from about 50 A to about 500 A [0019].

Regarding claim 27, AAPA teaches the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an Al_2O_3 layer and a TaON layer (page 2, line 22).

Regarding claim 28, AAPA teaches the cleaning process uses a cleaning solution of HF or BOE (page 5, line 9).

Regarding claim 29, AAPA teaches the conductive pattern **S** is a gate electrode pattern and the second plug **22** is a storage node contact plug (page 2, line 26 and page 8, line 9).

Response to Arguments

Applicant's arguments with respect to claims 1-29, 31, 32, and 36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,852,592, issued to Lee et al, discloses methods for fabricating semiconductor devices.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QVJ

QVJ

MICHELLE ESTRADA
PRIMARY EXAMINER